BEAMOS -- A NEW ELECTRON BEAM DIGITAL MEMORY DEVICE

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ABSTRACT

BEAMOS, for Beam Addressed Metal Oxide Semiconductor, is a new technology for auxiliary memories based on an electron beam which reads and writes data on a simple unstructured MOS chip. Its performance features include large bit capacity ($>30 \times 10^6$ bits/module), rapid access time (<30 microseconds), high data transfer rates, nonvolatile storage and low cost in comparison with memories of comparable performance. The memory component is rugged, all electronic, and relatively insensitive to temperature and vibration, making it especially attractive for military applications. Its fast access time should provide considerable performance improvement in both commercial and military computer systems.

INTRODUCTION

Most commercial computer systems employ discs or drums as auxiliary memories. These provide reasonably quick access to large quantities of information and provide a more cost effective system than would be achieved if a more expensive high speed memory were used. The access time for rotating magnetic memories is limited by the mechanical motion to many milliseconds, which is at least 10,000 times longer than for most main memory. Many computer systems are performance limited because of this long access time. In military systems, where the data base must be nonvolatile, thereby ruling out most semiconductor memories, discs and drums have the additional disadvantage of being unsuited for application in vehicular environments.

BEAMOS[1] is a new technology which offers improved performance in all of these respects. It is much faster than rotating mechanical memories, rugged enough for military applications, and less expensive than core or semiconductor. The BEAMOS module described here has a capacity of 32×10^6 bits and can be combined into systems with capacities larger than 600×10^6 bits. The system access time is less than 30 microseconds and the data transfer rate is from 10 to more than 200 megabits/second depending upon the number of modules and system organization.

THE BEAMOS COMPONENT

The BEAMOS memory module (Figure 1) has two major parts, an unstructured MOS memory plane, in which the data is stored as small islands of positive charge, and an electron beam accessing system for storage and retrival.

Memory Plane

The BEAMOS memory plane[2] (Figure 2) consists of a reverse biased n on p junction with an overlying MOS capacitor. The total oxide and aluminum layer thickness of 0.35 microns is thin enough to allow the 10 keV addressing electron beam to penetrate through into the n layer. The p substrate is lightly doped and the n layer is approximately 2 microns thick, 1 ohm-cm phosphorous doped.

Data is stored by biasing the aluminum layer positive with respect to the n layer and directing the electron beam to areas where ones are to be recorded. Hot electrons generated by the beam in the oxide are removed by the positive bias leaving a trapped layer of positive charge near the silicon electrode. Oxide fields as large as 5×10^6 volts/cm can be written by this method. Writing with the same beam voltage with 0 or negative bias erases the trapped charge.

The electron beam is also used for readout. The back biased diode of the memory plane acts as a current amplifier for the reading beam, providing a current gain which varies with the amount of charge stored at the addressed site.

Gain occurs because each electron penetrating into the n layer produces an electron hole pair for each 3.5 electron volts of beam energy, or approximately 1400 pairs/primary after energy loss in the oxide. If no charge is stored in the oxide, most of the minority carriers recombine with electrons at the silicon dioxide interface. Under regions where positive charge is stored, the surface recombination velocity is greatly reduced and most of the carriers reach the junction. The gain varies from approximately 100 where no charge is stored to about 1400 where there is charge. Each read operation removes some of the charge, but about 20 reads are possible before rewrite is necessary.

The writing data rate of the memory plane is limited by the available writing current in the device. For present modules, the writing current is 0.2 μA into a 2μ spot which gives a writing rate of 10 Mbits/sec. The frequency response of the target during read is not limited by the 1 MHz RC response of the diode capacitance and n layer resistance, as might be expected because at about 1 MHz the impedance of the oxide capacitance becomes small and the signal is coupled out of the top metal layer connection as displacement current. Figure 3 shows the calculated frequency response based on the distributed RC network shown in the figure. The signal to noise obtainable from such a structure using a voltage coupled amplifier can be shown to be:

$$S/N = \frac{\sqrt{3}}{2\pi f C} \quad \frac{i}{\langle E \rangle}$$

where f is the bandwidth, $\langle E \rangle$ the total rms voltage noise of the amplifier, C the total diode capacitance, and i the signal current generated by the target. This illustrates an important advantage of the BEAMOS target, that the signal is developed across a small capacitance (the diode capacitance) instead of the large oxide capacitance in which the information is recorded. Present devices operate at 10 Mbits/sec. with a signal to noise ratio of 15:1 at a reading beam current of 12 nA. As can be seen from the equation, small diode capacitance or higher signal current increases the signal to noise ratio. Larger signal current can be obtained by using a higher reading current. Reading currents up to 100 nA can be used with a proportionate reduction in the number of reads before refresh. Lower diode capacitance can be obtained by using small area targets or improving diode quality.

Electron Beam Access

The BEAMOS memory plane is accessed by means of an electron beam which is formed and controlled by a unique electron optical system[3] (Figure 4). The most important component in determining addressing accuracy is the matrix lens (Figure 5), which is an array of electron lens/deflection systems. The individual lenses are selectively illuminated from a single electron source by means of an electrostatic deflection device called the lenslet selector. The electrostatic deflection bars associated with the illuminated lenslet then address a particular data site within the lenslet. Because the optical system has high demagnification the two stages of deflection are decoupled, thereby greatly reducing the stability requirements for electronic deflection circuits. It has been demonstrated that such a matrix lens system can access more than 3×10^7 bits in a 1 inch square area using conventional electronics. No servoing to the desired data site is required. A system with comparable electronic accuracy, but using conventional single stage deflection would be limited to less than 10^6 bits.

The electron source makes use of a barium dispenser cathode with an expected life of 40 thousand hours[4].

BEAMOS MEMORY SYSTEMS

BEAMOS memory systems can be configured using one or more BEAMOS components together with the analog and digital circuitry indicated in Figure 6. As shown in the figure, multiple tube systems can share much of the circuitry resulting in a decrease in cost/bit for larger systems. The system illustrated in Figure 6 addresses one BEAMOS module at a time. Thus the data transfer rate is 10 Mbits sec. For higher data rates the system can be configured to address and read multiple modules in parallel without greatly increasing the electronics.

The access time to a data site is limited only by the speed of the deflection amplifiers and can be as low as a few microseconds. Thirty microseconds must be allowed for a switch in function, from read to write for example, to allow time for the oxide capacitance to be charged through the n layer resistance.

DEVELOPMENT STATUS

BEAMOS modules capable of storing 32 million bits and operating at 10 Mbits/sec. transfer rate and 30 microseconds access time

are being built in pilot quantities and are being operated in a computer controlled test system. Modules capable of 10^8 bits and similar transfer rates and access times have been operated successfully in limited test situations.

REFERENCES

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2. G. W. Ellis, G. E. Possin, and R. H. Wilson, "Diode Detection of Information Stored in Electron Beam-Addressed MOS Structure", Applied Physics Letters, 24, 419 (1974).
3. H. G. Parks and W. C. Hughes, "Advances in Matrix Lens Technology", Presentation at the 13th Symposium on Electron, Ion and Photon Beams, Colorado Springs, Colo., May 1975.
4. A. J. A. Van Stratum and P. N. Kuin, "Tracer Study of the Decrease of Emission Density of Osmium Coated Impregnated Cathodes", Journal of Applied Physics, 42, p. 4436 (1971).

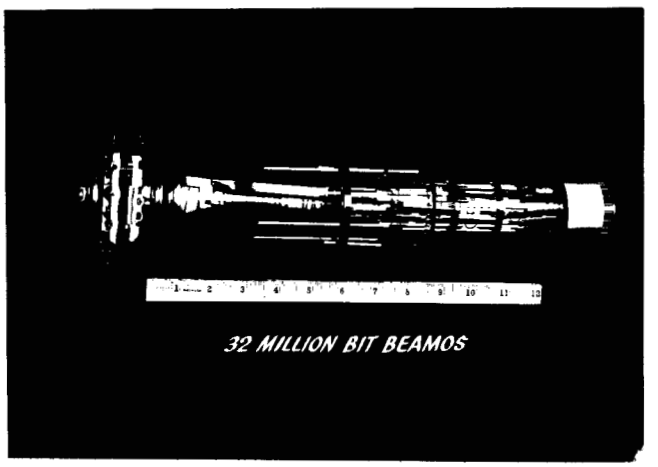

Fig. 1 BEAMOS memory component

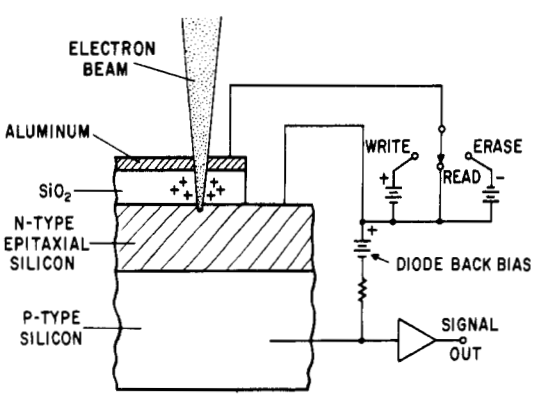

Fig. 2 Cross section of MOS memory chip

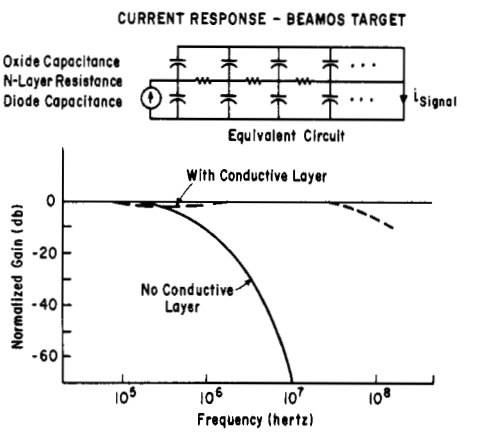

Fig. 3 Current Response -- BEAMOS Target

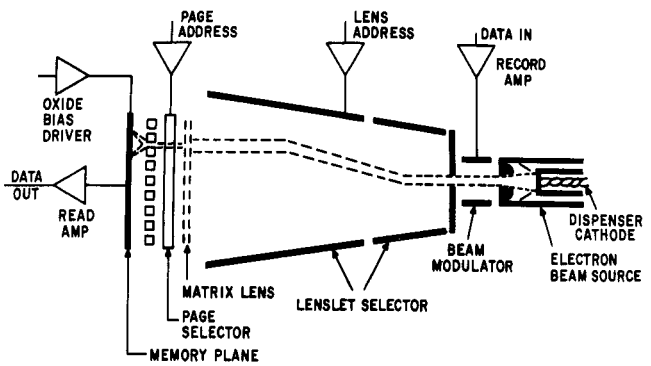

Fig. 4 BEAMOS electron optical system

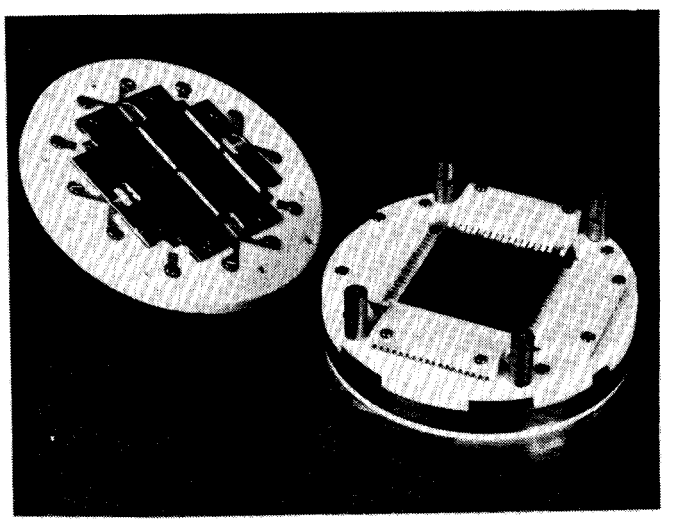

Fig. 5 Matrix lens with target plane removed showing page selector deflection bars

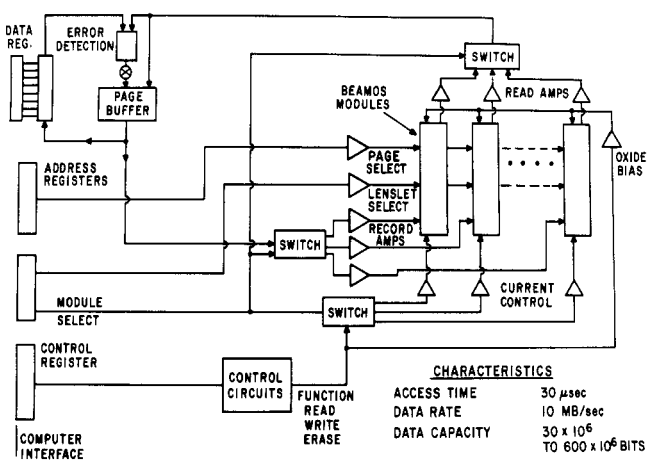

Fig. 6 Conceptual multimodule system - serial operation